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Multi bit Error Detection and Correction Architecture for Motion Estimation in Viedo Coding Systmes

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Abstract

The Motion Estimation (ME) is used in video coding systems to calculate the best motion between the current frame and reference frames. Process Element (PE) is the key component of ME. Error presence in the SAD value calculates by PE will affect the quality of the ME. In this paper the Built In Self Test (BIST) is used to test the PE this Error Detection and Correction Architecture (EDCA) designed based on the Residue and Quotient (RQ) code. Which will detect the multiple errors and recover the data with reduced delay from 16 clock cycles to 8 clock cycles.

Keywords: Motion Estimation, Process Element, Data recovery, error detection, residue-and-quotient (RQ) code.

Introduction

Motion Estimation (ME) is a process of determining Motion Vector (MV) which describe the transformation from reference frame to the current frame [1]. Usually adjacent frames in a video sequence, neighbor blocks in a frame will have very similar pixel colors and intensity [2]. In ME algorithm, Mean Square Error (MSE) and Sum of Absolute Differnce (SAD) estimation methods are used to identify the most similar block among the current reference frames [9]. SAD requires a simple calculation without the need for multiplications [3]. Regular arrangement of Process Elements (PEs) constitutes a ME. If an error is present in PE, it will effect the ME. So the testing of PE is essential to improve the quality of the video [1].

The complexity of VLSI chip increases testing time and complexity [4]. BIST is a Design For Testability (DFT) technique, where it makes the testing of a chip, board or system. It's implementation is easier, faster, efficient and less cost [5]. It is the technique of designing additional hardware and software features into integrated circuits to perform self-testing of PEs.

Various test Patterns can be applied to the internal nodes and response patterns are scanned out for comparison. The generalized block diagram of BIST is shown in Fig.1. Test Pattern Generator (TPG) is the combination of memory element which produces the test patterns inside the circuit itself. Response analysis also be done on-chip by Output Response Analyzer (ORA), where it with some additional logic produces a Pass/Fail signal [5].

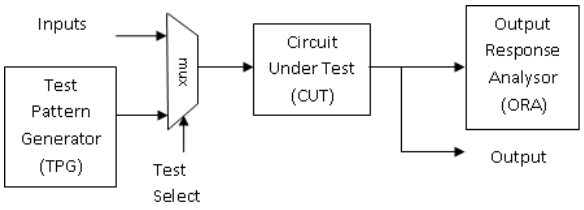

Fig. 1 Block Diagram of generalized BIST

Parity codes, Berger codes and Residue codes are used to detect and/or correct errors in the circuits. But these codes can detect only one bit error. If multiple errors are present in the data the residue code cannot detect the data effectively [6].

Residue code is a separable arithmetic code that estimates the residue of data and is appended to the data [7]. If N is an integer, N1 and N2 represents data words and 'm' refers to the modulus. Then N is coded as a pair (N_1, $|N|_m$), where $|N|_m$ is residue of N modulo m [1]. This residue coding approach can detect only one bit error. Therefore, a quotient code along with residue code is presented in this paper. Also detection and correction capabilities of these codes are analyzed in detail.

EDCA Design

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The Error Detection and Correction Architecture (EDCA) is shown in Fig. 2. The major blocks in the EDCA are Error Detection Circuit (EDC) and Data Recovery Circuit (DRC) to detect and correct the multiple errors in the PE.

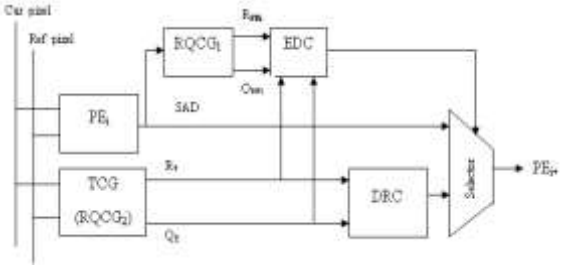

Fig. 2 EDCA architecture

PE is the circuit which is Circuit Under Test (CUT). The data generated by the PE is applied to Residue and Quotient Code Generator1 (RQCG1) to apply the RQ code to the data. The Test Code Generator (TCG) utilizes the Residue and Quotient (RQ) code concepts to generate the corresponding test code to detect the errors and also recover the data. The test codes from TCG and primary outputs of the PE are applied to EDC to determine whether the PE having error or not. The data can recover by DRC from TCG. Multiplexer (selector) is enabled to select the error free data or data recovery results.

A ME consists of many PEs incorporated in a 1-D or 2-D array for video encoding applications. The Internal block diagram of PE is shown in Fig. 3. PE consists of an 8-bit ADD and 12- bit Accumulator (ACC). The 8-bit ADD is used to estimate the addition of the current pixel (Cur_pixel) and reference pixel (Ref_pixel). 12-bit ACC is required to accumulate the results from the 8-bit ADD in order to determine the Sum of Absolute Difference (SAD) value for video encoding applications (Chang-Hsin Cheng et al 2012).

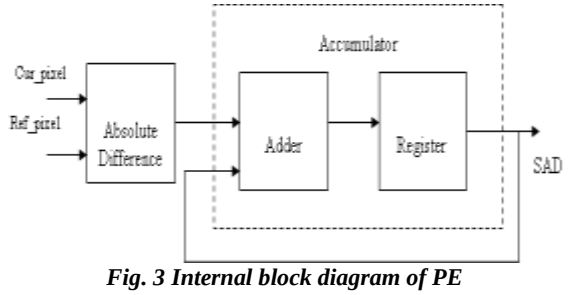

Fig. 3 Internal block diagram of PE

A sample of the 16 pixels is taken as an example and the pixel values are shown in Fig.4 with 4X4 macro block (Chang-Hsin Cheng et al 2012). The SAD value of the 4x4 macro block is given as [10]:

	0	1	2	3
0	128	128	64	255
1	128	64	255	64
2	64	255	64	128
3	255	64	128	128

a.Cur_pixel

	0	1	2	3
0	1	1	2	3
1	1	2	3	4
2	2	3	4	5
3	3	4	5	5

b. Ref_pixel

Fig. 4 Examples of pixel values

$$SAD = \sum_{i=0}^{N-1}\sum_{j=0}^{N-1}|X_{ij} - Y_{ij}| \quad (1)$$

$$= |X00 - Y00| + |X01 - Y01| + \ldots + |X33 - Y33|$$

$$= (128 - 1) + (128 - 1) + \ldots\ldots + (128 - 5)$$

$$= 127 + 127 + \ldots\ldots + 123 = 2124$$

Residue and Quotient Code Generation

RQ code can detect multiple bit errors. It can be generated with low complexity and less hardware cost. The mathematical model of RQ code is as follows. Assume X is the binary data which can be expressed as

$$X = \{b_{n-1}b_{n-2}\ldots\ldots b_2 b_1 b_0\} = \sum_{j=0}^{n-1} b_j 2^j \quad (2)$$

The RQ code for X modulo m is expressed as

$$R = |X|_m \quad (3)$$

$$Q = \lfloor X/m \rfloor \quad (4)$$

Where m can be calculated as $2^k - 1$ where k is n/2 therefore $m=2^6-1=63$. The SAD value generated by PE is the input to the RQCG. RQ code for 2124 is $R_{PEi} = |2124|63 = 45$ and $Q_{PEi} = |2124/63| = 33$.

Test Code Generation (TCG)

TCG is the main block of the EDCA design. The block diagram of TCG is as shown in Fig. 5.

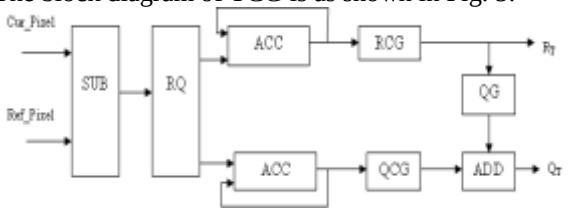

Fig. 5 Block diagram of TCG

Which is designed based on the ability of the RQCG circuit to generate corresponding codes in order to detect errors and recover the data. The circuit design of TCG is achieved by the following equation (5) and (6)

$$R_T = \left|\sum_{i=0}^{N-1}\sum_{j=0}^{N-1}(X_{ij} - Y_{ij})\right| m$$

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$$= \left|\left|X_{00} - Y_{00}\right|m + \left|X_{01} - Y_{01}\right|m + \cdots + \left|X_{(N-1)(N-1)} - Y_{(N-1)(N-1)}\right|m\right| m$$
$$= |r_{00} + r_{01} + \cdots + r_{(N-1)(N-1)}|m \quad (5)$$
$$= 45$$

$$Q_T = \left\lfloor \frac{\sum_{i=0}^{N-1}\sum_{j=0}^{N-1}(X_{ij} - Y_{ij})}{m} \right\rfloor$$
$$= \left\lfloor \frac{(X_{00}-Y_{00})+(X_{01}-Y_{01})+\cdots+(X_{(N-1)(N-1)}-Y_{(N-1)(N-1)})}{m} \right\rfloor$$
$$= q_{00} + q_{01} + \cdots + q_{(N-1)(N-1)} + \left\lfloor \frac{r_{00} + r_{01} + \cdots + r_{(N-1)(N-1)}}{m} \right\rfloor \quad (6)$$
$$= 33$$

Error Detection Process

Error Detection Circuit (EDC) is works as an output response analyzer. It will detects whether the error present or not in the specific PE as shown in Fig. 6. This block is used to compare the output from TCG i.e., R_T and Q_T with output from RQCG1 i.e., R_{PEi} and Q_{Pei} to detect the occurrence of an error.

The logic diagram of EDC is shown in Fig. 7. If the value of $R_{PEi} \neq R_T$ and/or $Q_{PEi} \neq Q_T$ then the error in the PEi can be detected by EDC. Output is then generated as a 0/1 signal to indicate that the tested PE_i is error free/ with error

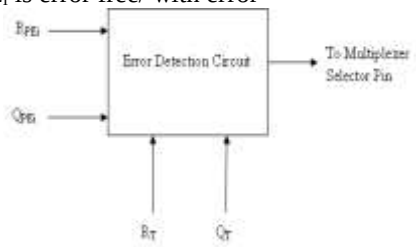

Fig. 6 Block diagram of EDC

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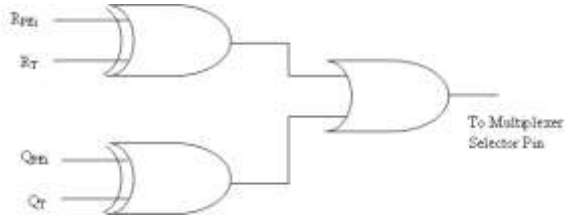

Fig. 7 Logic diagram of EDC

Fault Model

In practical approach to test circuits select a specific test patterns based on circuit structural information and a set of fault models [1]. The structural fault model which assumes that faults cause line in the circuit to behave as if t were permanently at logic "0" (stuck-at 0 (SA0)) or logic "1" (stuck-at1(SA1)) [8]. The Stuck-at model, must be adopted to cover actual failures in the interconnect data bus between PEs. The structural tsting in ME architecture can incur error in computing SAD values.

If we introduce stuck-at faults in the SAD value of PE_i, 2124 = (100001001100)2 as SA1 at bit1 and SA0 at bit 12 of the SAD value. Then the value is turned into 77= (000001001101)2, resulting in the transformation of the RQ code of R_{PEi} and Q_{PEi} into |77|=14and $\lfloor 77/63 \rfloor = 1$.

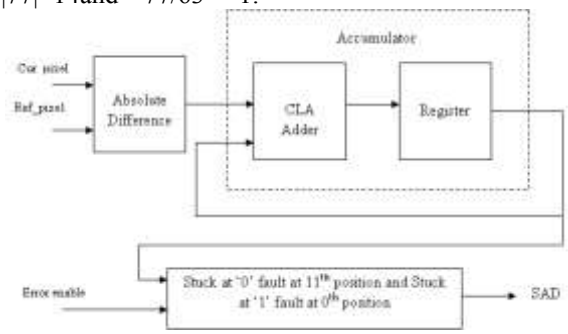

Fig. 8 Error introduction Logic Diagram

Data Recovery Circuit

During error correction process the RQ code is separated from the TCG and the original data can be recovered by Data Recovery Circuit (DRC). The data recovery is possible by implementing the following mathematical model.

$$SAD = m \times Q_T + R_T$$
$$= (2^k - 1) \times Q_T + R_T$$
$$= 2^k \times Q_T - Q_T + R_T \quad (7)$$

The EDCA design executes the error detection and data recovery operations simultaneously, additionally the error free data are passed to the next specific PE_{i+1} through the multiplexer. The multiplexer will select the error free data from the tested PE_i or the data recovery results from DRC.

Results and discussion

The EDCA design is developed in a top down design methodology using Xilinx 13.2 with VHDL coding. The top down design methodology is code mixed version of both behavioral and structural. The architecture consists of basic modules like Process element, TCG, RQ code generator, Multiplexer, EDC and DRC modules.

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The behavioral simulation result for Top module without error introduced is shown in fig. 9. From the figure we can observe that the of $R_{PEi} = R_T$ and/or $Q_{PEi} = Q_T$ so the SAD value calculated by the PE_i is applied to the next PE. The delay for the SAD value calculation is 16 clock cycles.

Fig. 9 Behavioral simulation result for Top module without error introduced

The behavioral simulation result for Top module with error introduced is shown in fig. 10. From the figure we can observe that the of $R_{PEi} \neq R_T$ and/or $Q_{PEi} \neq Q_T$ so the error in SAD value calculated by the PE_i is detected by the EDC and the output form DRC is applied to the next PE. Which is the data recovered from the R_T and Q_T. The RTL Schematic view of top module is shown in Fig. 11.

Fig. 10 Behavioral simulation result for Top module with error introduced

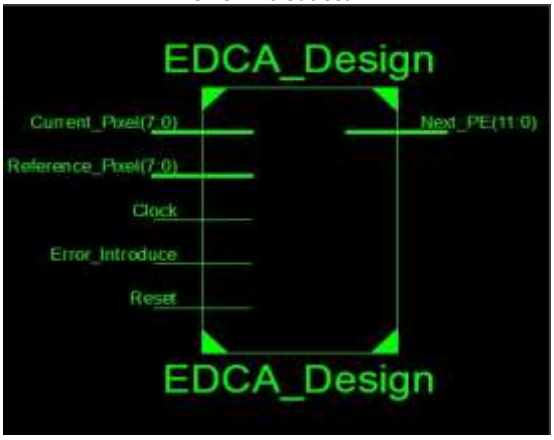

Fig. 11 RTL Schematic of Top module

The delay can be reduced by using two Process Elements and two TCG blocks instead of one. The delay will become half that is, it will become 8 clock cycles. Fig. 12 show the behavioral simulation result for the top module with delay reduced.

Fig. 12 Behavioral simulation result for Top module with delay reduced

Conclusion

In motion estimation process of finding the motion vector pointing to the best prediction macroblock in a reference frame or field. An error occurred in the ME will degrade the quality of the video. PE is the basic block in the MV calculation. This EDCA design will detect the multiple errors occurred in the PE and recover the data with less time delay.

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